et al (U.S. Patent No. 6,130,454A) and Hsu et al (U.S. Patent No. 6,221,767B1) and Brigham et al ('413).

Claims 1 through 18 remain in the application. No claims are amended herein. No claims are cancelled. No claims are added. Accordingly, Claims 1 through 18 remains pending.

**CLAIM REJECTIONS- 35 U.S.C. SECTION 103 (a)**

With respect to Page 2 through Page 7 of the Office Action, the Examiner rejected Claims 1-8 under 35 U.S.C. Section 103 (a) as being unpatentable over Gardner et al ('454) and Hsu et al ('767); and Claims 9-18 under 35 U.S.C. Section 103(a) as being unpatentable over Gardner et al ('454), Hsu et al ('767), and Brigham et al ('413). Of the rejected claims, only Claims 1and 9 are independent.

Applicant respectfully traverses these rejections.

The Examiner is of the opinion that Gardner et al ('454) teaches a method of forming a MOSFET, but fails to teach activation of source/drain implanted ions by rapid heating as recited in present claim 1. However, the Examiner alleges that is well known to one skilled in the art that rapid heating has been used in activating ion-implanted regions because rapid heating reduces unwanted heat exposure to the device. In addition, Examiner agrees that Gardner et al fails explicitly teach the removal of unwanted metal after the silicidation process as recited in present claim. Nevertheless, the Examiner alleges that Hsu et al teaches that unwanted metal formed during the silicidation process is removed.

Gardner et al discloses that dielectric spacers (32) are formed adjacent the opposed lateral boundaries of nitride layer and the opposed sidewalls of trench (FIG. 9) (herein named the reference number 32 as the first spacer), and further Gardner et al discloses another dielectric sidewall spacer (herein named the reference number 53 as the second spacer) formed such that they extend laterally from the opposed sidewall surfaces of gate conductor (col. 8, line 67-col. 9, line 3, and FIG. 12. Nevertheless, the position of the spacer on the trench is different between FIG. 6 and FIG. 12 of Gardner et al and the FIG.9 of the present invention. The present invention **ONLY** forms **a spacer on the sidewalls of the gate** (page 26 of the specification). Referring to Gardner et al, the first spacer (reference number 32) is formed on the "**opposed lateral boundaries of nitride layer and the opposed sidewall the trench"**.

Furthermore, Gardner et al discloses that the first spacer is to be removed "**after**" the gate conductor is formed (col. 7, line 44-47). The present invention recites that the gate is **first** formed on the trench, and the spacer is **then** formed on the sidewall of the gate (FIG. 7 to FIG. 9). According to the well-known fabrication of semiconductors, if the spacer is formed on the sidewall of the gate as the present invention recites, so **the gate should be first formed on the trench, then, the spacer will form on the sidewall of the gate**. Thus, the formation for gate and spacer cannot be reversed in the present invention. Thus, the forming step of the spacer and gate are different between Gardner et al and the present invention.

Moreover, Gardner et al discloses that the second sidewall spacer is formed such that they extend laterally from the opposed sidewall surfaces of gate conductor. The purpose of the second sidewall spacer is to help prevent silicide from forming laterally adjacent gate conductor (col. 8, line 67- col. 9, line 4). The **second sidewall spacer is formed "after" the implantation process for forming LDD region and source/drain region**. Nevertheless, the present invention recites the **spacer is formed on the sidewall of the gate, then the implantation process is performed to form the source/drain region and the first rapid thermal process (RTP) proceeds to be the anneal process**. Thus, the depth of ions and the temperature of the RTP process are controlled to make the ions, which are implanted, move to the suitable place by way of diffusion and the permeation to form the source/drain extended region. Thus, **the forming step of the LDD region and the source/drain region is formed "before" the second sidewall spacer that differs from the source/drain region and the source/drain extended region is formed "after" the spacer that is formed.**

In addition, Gardner et al discloses the LDD areas are shallower than and have a lower concentration of dopants than source and drain region, and the S/D implant is performed at a higher dose and energy than the LDD implant (col. 8, lines 37-39 and line 48-49). Referring to FIG. 9a of Gardner et al, the LDD areas with higher dopants concentration is first formed in the substrate and adjacent the trench, then the source/ drain region with lower concentration than the LDD areas that is formed both LDD areas proximate the trench sidewalls and source/drain region (col. 8, line 34-36).

In the present invention, the source/drain region is first formed in the substrate, then performing a first RTP process to form the source/drain extended region. Therefore, the forming step is different between LDD areas and the source/drain region as Gardner et al disclose and the source/drain region and the source/drain extended region as the present invention recites.

Moreover, as regards the present invention, the source/drain extended region is formed **"below"** the source/drain (referring to FIG. 10). Nevertheless, Gardner et al discloses the LDD areas "adjacent" the sidewall of the trench and on **"above"** the source/drain region (referring to FIG. 10b). Thus, the positional relationship is different between the source/drain region and the LDD region as Gardner et al discloses and the source/drain region and source/drain extended region as the present invention recites. Thus, the combination of Gardner et al, Hsu et al, and Brigham et al cannot achieve the present invention.

**Conclusion**

In light of the above remarks, Applicants respectfully submit that all pending Claims 1 through 18 as currently presented are in condition for allowance. Accordingly, reconsideration is respectfully requested.